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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
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EXAMINER: F 003057 P003D

TM02/0405

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ART UNIT: BUTLER, D | PAPER NUMBER: 15

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This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☒ Responsive to communication(s) filed on 1-29-01

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire three month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 34-74 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 34-74 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of Reference Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

– SEE OFFICE ACTION ON THE FOLLOWING PAGES –

1. This action is in response to paper number 10, Amendment C, which was received on December 27, 2000.

2. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

3. In the remarks applicant stated that a terminal disclaimer was submitted with amendment C. However, a terminal disclaimer was not attached to amendment C and the Terminal Disclaimer box on applicant's Transmittal Form was not checked. The terminal disclaimer was not received and it is not present in applicant's file.

4. The non-statutory double patenting rejection, whether obviousness-type or non-obviousness-type, is based on a judicially established doctrine grounded in public policy (a policy reflected in a statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent. In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); In re Van Ornam, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); and In re Goodman, 29 USPQ2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer in compliance with 37 CFR § 1.321(b) and (c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR § 1.78(d).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer

signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 34-74 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 7-30 of U.S. patent no. 5,802,398. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are directed to substantially the same invention where the disk drive corresponds to the first storage device, the tape drive corresponds to the second storage device and the interface corresponds to the IDE interface. Claims 35-45 and 66-74 of the application correspond to claims 15-22 of the patent. Claims 46-50 of the application correspond to claims 23-26 of the patent. Claims 51-56 of the application correspond to claims 27-30 of the patent. Claims 57-65 of the application correspond to claims 7-14 of the patent. The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter. Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. In Re Schneller, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

6. Claims 34-74 are rejected under 35 USC 103 as being unpatentable over Klashka et al, U.S. Patent 4,803,623 in view of applicant's admissions.

Per claims 34, 40 and 66:

A) Klashka teaches the following claimed items:

1. a buffer management means with UPC 209 of figure 2 and a memory buffer with adapter 212 of figure 2; Klashka further describes that adapters are used to connect tape drives to controller 209 and that adapters include memory buffering circuitry (registers) for data buffering with figure 2 and at column 5, lines 59-64;
2. a storage medium with the storage medium of the tape peripheral and/or the disk peripheral;
3. a controller circuit with Universal Peripheral Controller 209 and Adapters 212 of figure 2, at column 5, lines 46-64 and at column 12, lines 15-17.

B) The claims seem to differ from Klashka in that Klashka fails to explicitly teach the IDE interface as claimed.

C) However, by applicant's own admission on pages 2-3 of the specification, IDE controllers were known in the art, available on the market and used to interface disk drives at the time of the invention. Therefore, it would have been obvious for one of ordinary skill in the art to use an IDE controller in order to interface a storage device with a separate storage device.

Per claims 35-39, 41-45 and 67-74:

Klashka describes a hard disk device with Disk Peripheral 214 of figure 2 and a tape drive device with Tape Peripheral 213 of figure 2. Klashka describes that adapters are used to connect tape drives to controller 209 which include circuitry for buffering, synchronization and error detection with figure 2 and at column 5, lines 59-64. Klashka

describes indicating whether the tape drive device is receiving information over the interface with the data channel busy indication, with figures 5A and 7Q, at column 5, lines 32-34, at column 7, lines 1-14, 30-36 and 48-51 and at column 20, lines 37-65. Klashka describes first indicator means indicating whether the first storage device is executing a command with the address channel busy indication and the address channel ACK indication at column 12, lines 34-59. Klashka describes second indicator means indicating whether the second storage device is receiving information over the interface with the data channel busy indication, with figures 5A and 7Q, at column 5, lines 32-34, at column 7, lines 1-14, 30-36 and 48-51 and at column 20, lines 37-65.

Per claims 46 and 57:

A) Klashka teaches the following claimed items:

1. a buffer management means with UPC 209 of figure 2 and a buffer with adapter 212 of figure 2; Klashka further describes that adapters are used to connect tape drives to controller 209 which include circuitry for buffering, synchronization and error detection with figure 2 and at column 5, lines 59-64;
2. a storage medium with the storage medium of the tape peripheral and/or the disk peripheral;
3. an interface with Universal Peripheral Controller 209 and Adapters 212 of figure 2 and at column 5, lines 46-64;
4. a first circuit and a second circuit with adapter 212 and at

column 5, lines 25-38 and 46-64;

5. a third circuit with UPC 209 of figure 2, at column 5, lines 25-38 and at column 7, lines 1-51.

B) The claims seem to differ from Klashka in that Klashka fails to explicitly teach the IDE interface as claimed.

C) However, by applicant's own admission on pages 2-3 of the specification, IDE controllers were known in the art, available on the market and used to interface disk drives at the time of the invention. Therefore, it would have been obvious for one of ordinary skill in the art to use an IDE controller in order to interface a storage device with a separate storage device.

Per claims 47-50 and 58-65:

Klashka describes a hard disk device with Disk Peripheral 214 of figure 2 and a tape drive device with Tape Peripheral 213 of figure 2. Klashka describes providing priority based communication and transmitting commands and addresses at column 5, lines 25-64. Interrupt signals are well known control signals and it would have been obvious to generate interrupt signals in order to control communication between a host computer and an interface.

Per claim 51:

A) Klashka teaches the following claimed items:

1. a host computer with figure 1;

2. an interface with Universal Peripheral Controller 209 and Adapters 212 of figure 2 and at column 5, lines 46-64;

3. a first storage device with Drive 408B of figure 4B;

4. a second storage device with Drive 409B of figure 4B;

5. a storage medium with the storage medium of the tape peripheral of figure 4B;

6. a buffer management means with UPC 209 of figure 2 and a buffer with adapter 212 of figure 2; Klashka further describes that adapters are used to connect tape drives to controller 209 which include circuitry for buffering, synchronization and error detection with figure 2 and at column 5, lines 59-64;

7. control circuitry with UPC 209 of figure 2, at column 5, lines 25-38 and at column 7, lines 1-51.

B) The claims seem to differ from Klashka in that Klashka fails to explicitly teach the only one device being able to communicate with the host computer over the interface as claimed.

C) However, Klashka describes that UPC 209 has four ports which allows four simultaneous data transfers at column 5, lines 25-38. However, it would clearly have been obvious to one of ordinary skill in the art that the UPC could be modified to include only a single port which would allow only one device to communicate with the host computer over the interface in order to reduce the circuitry, size and cost of the UPC.

Per claims 52-56:

Klashka describes a hard disk device with Disk Peripheral 214 of figure 2 and a tape drive device with Tape Peripheral 213 of figure 2. By applicant's own admission on pages 2-3 of the specification, IDE controllers were known in the art,

available on the market and used to interface disk drives at the time of the invention. Therefore, it would have been obvious for one of ordinary skill in the art to use an IDE controller in order to interface a storage device with a separate storage device. Klashka describes providing priority based communication and transmitting commands and addresses at column 5, lines 25-64. Interrupt signals are well known control signals and it would have been obvious to generate interrupt signals in order to control communication between a host computer and an interface.

7. In the remarks, applicants argued in substance that:

A) applicant provided remarks regarding the examiner's understanding of the claimed IDE interface as being the IDE interface that was known at the time of applicant's invention. Applicant has cited MPEP § 2111 and argued that the examiner must give the claimed IDE interface the broadest reasonable interpretation consistent with the specification. Applicant further argues that the claimed elements and limitations are applicable to different standards of the IDE interface.

B) Klashka does not disclose a controller circuit that allows for simultaneous transfers of data from a buffer to a storage medium for a given storage device while a separate storage device transmits and/or receives on the same interface.

C) Klashka does not disclose a system wherein an interface is released prior to the completion of a data transfer to the storage medium for a given device.

8. As to point A, the examiner disagrees with applicant's

contentions. The examiner did give the claimed IDE interface the broadest reasonable interpretation consistent with the specification. The term "IDE" is a trade name describing an industry standard which is revised from year to year. This case was originally filed on November 13, 1990, over ten years ago. The examiner requested applicant to recited a specific version of the IDE standards used in the claimed invention. Applicant chose not to amend the claims to include the version. Therefore, in this application, the examiner continues to understand the claimed IDE interface as being the IDE interface or interfaces that were known at the time of applicant's invention. Regarding the broadest reasonable interpretation consistent with the specification, the examiner can not apply art to the claimed invention that was published or filed with the Office after applicant's filing date of November 13, 1990. See MPEP § 706.02 and 706.02(a). In addition, the MPEP states that an application must be complete at the time of filing and that no new matter may be introduced into an application after its filing date. See MPEP § 601.01. Therefore, it is clearly not reasonable to interpret the claimed IDE interface as one of the interfaces that conforms to IDE standards that were developed after applicant's filing date because applicant has not described or enabled such an IDE interface and there is no prior art that could possibly be applied to such an interface.

As to point B, the examiner disagrees with applicant's contentions. The claim language of claim 34 does not recite "simultaneous transfers" as described in the arguments but

recites "simultaneous at least in part". Therefore, it is irrelevant whether Klashka describes the above function because the above function is not being claimed. In addition, Klashka does describe transferring data simultaneous at least in part as claimed at column 12, lines 15-17.

Regarding claims 40-45, applicant failed to provide any arguments directed to these claims. However, these claims are similar to claims 34-39 and the remarks directed to claims 34-39 may apply to claims 40-45.

As to point C, Klashka describes providing each adapter with a data buffer at column 5, lines 59-64. Klashka also describes that UPC 209 provides for four levels of simultaneity (i.e., four data transfers can be active in the subsystem) at column 12, lines 15-17. Filling a buffer with a block of data in order to reduce the time required for an interface to process a block of data and release an interface for further processing is an obvious use of a data buffer.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is (703) 305-9663. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Dennis M. Butler
April 3, 2001

Dennis M. Butler
Primary Examiner
Group 2180